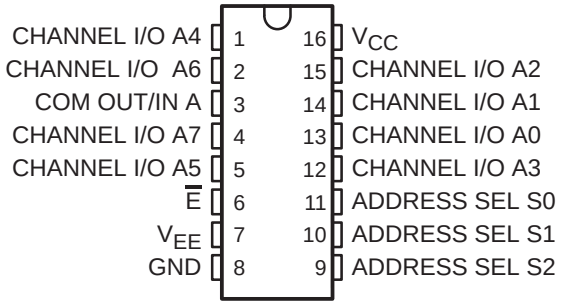
- **Qualification in Accordance With AEC-Q100†**
- **Qualified for Automotive Applications**
- **Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval**
- **Wide Analog Input Voltage Range of ±5 V Max**
- **Low ON Resistance**
  - **70 Ω Typical (V_{CC} − V_{EE} = 4.5 V)**
  - **40 Ω Typical (V_{CC} − V_{EE} = 9 V)**
- **Low Crosstalk Between Switches**
- **Fast Switching and Propagation Speeds**
- **Break-Before-Make Switching**

† Contact factory for details. Q100 qualification data available on request.

- **Operation Control Voltage = 2 V to 6 V**
- **Switch Voltage = 0 V to 10 V**
- **High Noise Immunity N_{IL} = 30%, N_{IH} = 30% of V_{CC}, V_{CC} = 5 V**

M OR PW PACKAGE
(TOP VIEW)



description/ordering information

This device is a digitally controlled analog switch that utilizes silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

This analog multiplexer/demultiplexer controls analog voltages that may vary across the voltage supply range (i.e., V_{CC} to V_{EE}). These bidirectional switches allow any analog input to be used as an output and vice versa. The switches have low ON resistance and low OFF leakages. In addition, the device has an enable control ($\overline{E}$) that, when high, disables all switches to their OFF state.

ORDERING INFORMATION

T_A	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 125°C	SOIC − M	Tape and reel	CD74HC4051QM96Q1	HC4051Q
	TSSOP − PW	Tape and reel	CD74HC4051QPWRQ1	HJ4051Q

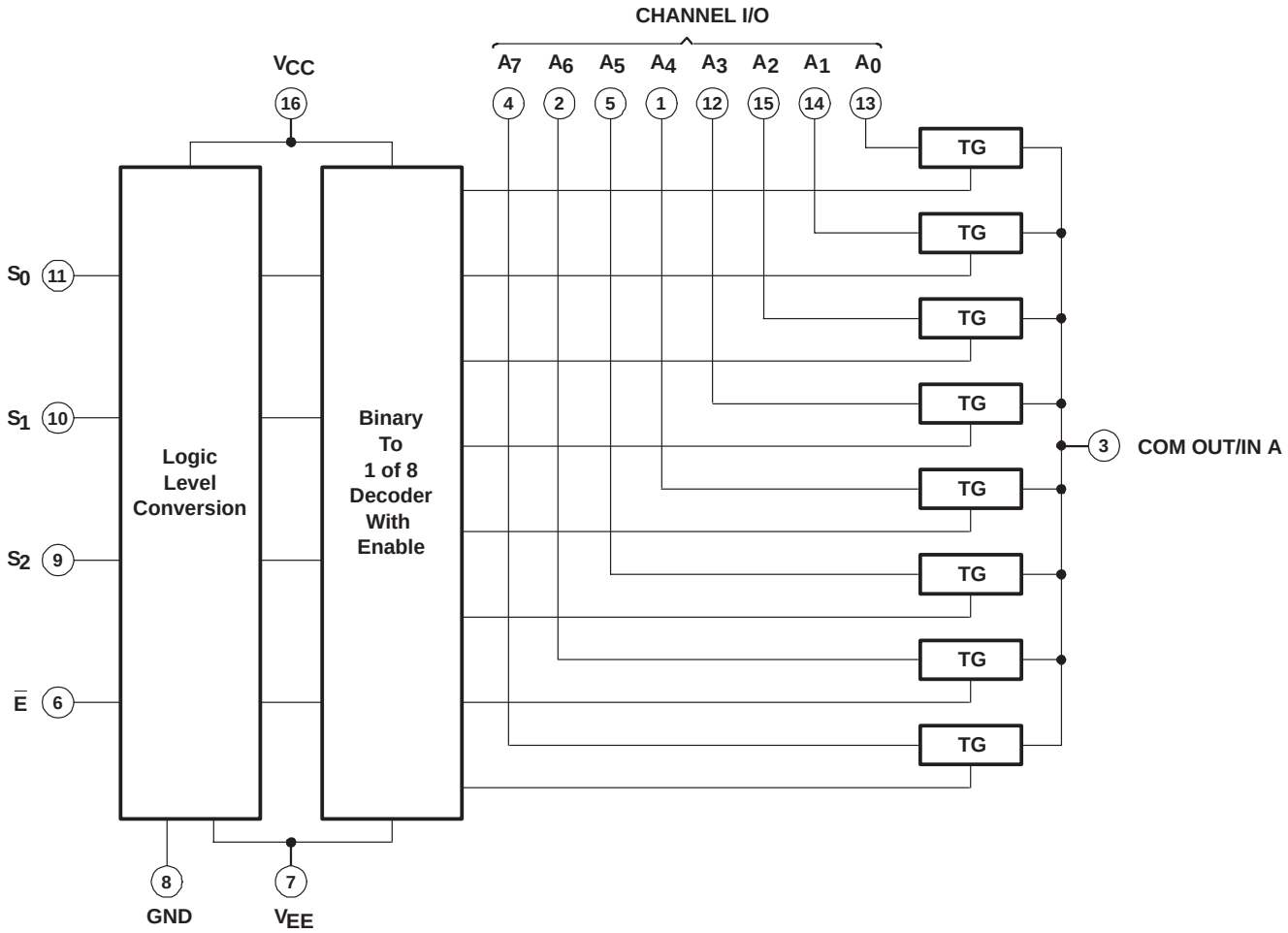
‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPUTS				ON CHANNEL(S)
$\overline{E}$	S_2	S_1	S_0	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

X = Don't care

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} − V_{EE} (see Note 1) . . . . . −0.5 V to 10.5 V
Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Supply voltage range, V_{EE} . . . . . +0.5 V to −7 V
Input clamp current, I_{IK} (V_I < −0.5 V or V_I > V_{CC} + 0.5 V) . . . . . ±20 mA
Output clamp current, I_{OK} (V_O < V_{EE} − 0.5 V or V_O > V_{CC} + 0.5 V) . . . . . ±20 mA
Switch current (V_I > V_{EE} − 0.5 V or V_I < V_{CC} + 0.5 V) . . . . . ±25 mA
Continuous current through V_{CC} or GND . . . . . ±50 mA
V_{EE} current, I_{EE} . . . . . −20 mA
Package thermal impedance, θ_{JA} (see Note 2): M package . . . . . 73°C/W
PW package . . . . . 108°C/W
Maximum junction temperature, T_J . . . . . 150°C
Lead temperature (during soldering):
At distance 1/16 ± 1/32 inch (1,59 ± 0,79 mm) from case for 10 s max . . . . . 300°C
Storage temperature range, T_{stg} . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltages referenced to GND unless otherwise specified.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			MIN	MAX	UNIT
V_{CC}	Supply voltage (see Note 4)		2	6	V
	Supply voltage, V_{CC} − V_{EE} (see Figure 1)		2	10	V
V_{EE}	Supply voltage, (see Note 4 and Figure 2)		0	−6	V
V_{IH}	High-level input voltage	V_{CC} = 2 V	1.5		V
		V_{CC} = 4.5 V	3.15		
		V_{CC} = 6 V	4.2		
V_{IL}	Low-level input voltage	V_{CC} = 2 V		0.5	V
		V_{CC} = 4.5 V		1.35	
		V_{CC} = 6 V		1.8	
V_I	Input control voltage		0	V_{CC}	V
V_{IS}	Analog switch I/O voltage		V_{EE}	V_{CC}	V
t_t	Input transition (rise and fall) time	V_{CC} = 2 V	0	1000	ns
		V_{CC} = 4.5 V	0	500	
		V_{CC} = 6 V	0	400	
T_A	Operating free-air temperature		−40	125	°C

NOTES: 3. All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
4. In certain applications, the external load resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6 V (calculated from r_{on} values shown in electrical characteristics table). No V_{CC} current flows through R_L if the switch current flows into the COM OUT/IN A terminal.

recommended operating area as a function of supply voltages

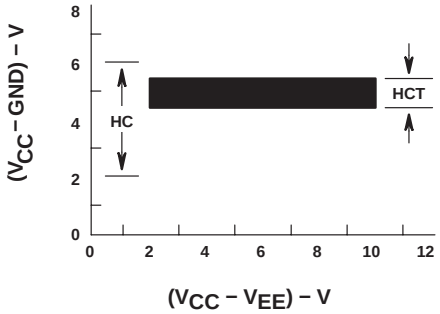


Figure 1

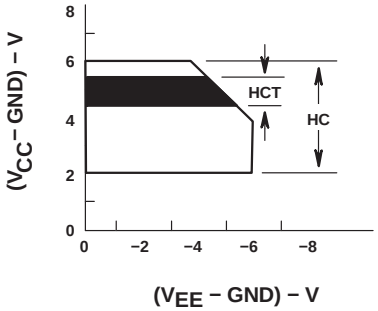


Figure 2

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{EE}	V_{CC}	T_A = 25°C			T_A = −40°C TO 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
r_{on}	I_O = 1 mA, V_I = V_{IH} or V_{IL}, See Figure 8	V_{IS} = V_{CC} or V_{EE}	0 V	4.5 V		70	160		240	Ω
			0 V	6 V		60	140		210	
			−4.5 V	4.5 V		40	120		180	
		V_{IS} = V_{CC} to V_{EE}	0 V	4.5 V		90	180		270	
			0 V	6 V		80	160		240	
			−4.5 V	4.5 V		45	130		195	
Δr_{on}	Between any two channels		0 V	4.5 V		10				Ω
			0 V	6 V		8.5				
			−4.5 V	4.5 V		5				
I_{IZ}	For switch OFF: When V_{IS} = V_{CC}, V_{OS} = V_{EE}; When V_{IS} = V_{EE}, V_{OS} = V_{CC} For switch ON: All applicable combinations of V_{IS} and V_{OS} voltage levels, V_I = V_{IH} or V_{IL}		0 V	6 V			±0.2		±2	µA
			−5 V	5 V			±0.4		±4	
I_{IL}	V_I = V_{CC} or GND		0 V	6 V			±0.1		±1	µA
I_{CC}	I_O = 0, V_I = V_{CC} or GND	When V_{IS} = V_{EE}, V_{OS} = V_{CC}	0 V	6 V			8		160	µA
		When V_{IS} = V_{CC}, V_{OS} = V_{EE}	−5 V	5 V			16		320	

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 7)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{EE}	V_{CC}	T_A = 25°C			T_A = −40°C TO 125°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
t_{pd}	IN	OUT	C_L = 15 pF		5 V		4				ns
			C_L = 50 pF	0 V	2 V			60		90	ns
					4.5 V			12		18	
					6 V			10		15	
				−4.5 V	4.5 V			8		12	
t_{en}	ADDRESS SEL or $\overline{E}$	OUT	C_L = 15 pF		5 V		19				ns
			C_L = 50 pF	0 V	2 V			225		340	
					4.5 V			45		68	
					6 V			38		57	
				−4.5 V	4.5 V			32		48	
t_{dis}	ADDRESS SEL or $\overline{E}$	OUT	C_L = 15 pF		5 V		19				ns
			C_L = 50 pF	0 V	2 V			225		340	
					4.5 V			45		68	
					6 V			38		57	
				−4.5 V	4.5 V			32		48	
C_I	Control		C_L = 50 pF					10		10	pF

operating characteristics, V_{CC} = 5 V, T_A = 25°C, Input t_r, t_f = 6 ns

PARAMETER		TYP	UNIT
C_{pd}	Power dissipation capacitance (see Note 5)	50	pF

NOTE 5: C_{pd} is used to determine the dynamic power consumption, per package.
$P_D = C_{pd} V_{CC}^2 f_I + \Sigma (C_L + C_S) V_{CC}^2 f_O$
f_O = output frequency
f_I = input frequency
C_L = output load capacitance
C_S = switch capacitance
V_{CC} = supply voltage

analog channel characteristics, T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{EE}	V_{CC}	MIN	TYP	MAX	UNIT
C_I	Switch input capacitance					5		pF
C_{COM}	Common output capacitance					25		pF
f_{max}	Minimum switch frequency response at −3 dB	See Figure 3 and Figure 9, and Notes 6 and 7	−2.25 V	2.25 V		145		MHz
			−4.5 V	4.5 V		180		
	Sine-wave distortion	See Figure 4	−2.25 V	2.25 V		0.035		%
			−4.5 V	4.5 V		0.018		
	$\overline{E}$ or ADDRESS SEL to switch feed-through noise	See Figure 5, and Notes 7 and 8	−2.25 V	2.25 V		(TBD)		mV
			−4.5 V	4.5 V		(TBD)		
	Switch OFF signal feed through	See Figure 6 and Figure 10, and Notes 7 and 8	−2.25 V	2.25 V		−73		dB
			−4.5 V	4.5 V		−75		

NOTES: 6. Adjust input voltage to obtain 0 dBm at V_{OS} for f_{IN} = 1 MHz.
7. V_{IS} is centered at $(V_{CC} - V_{EE})/2$.
8. Adjust input for 0 dBm.

PARAMETER MEASUREMENT INFORMATION

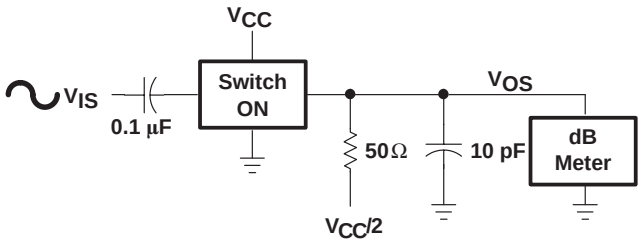


Figure 3. Frequency-Response Test Circuit

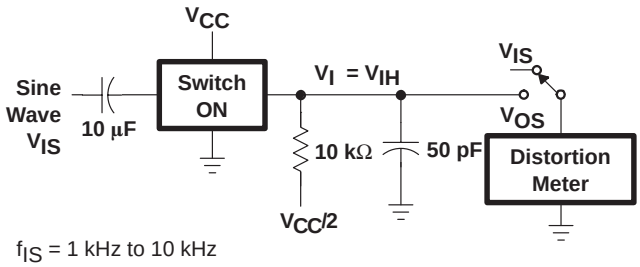


Figure 4. Sine-Wave Distortion Test Circuit

PARAMETER MEASUREMENT INFORMATION

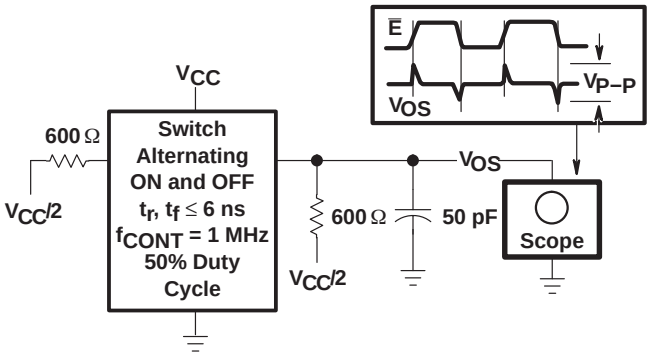


Figure 5. Control to Switch Feedthrough Noise Test Circuit

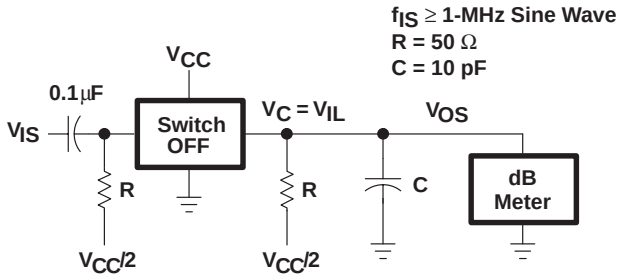
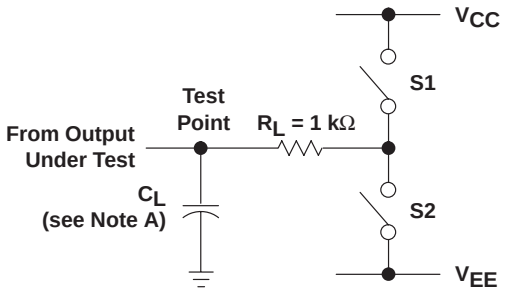


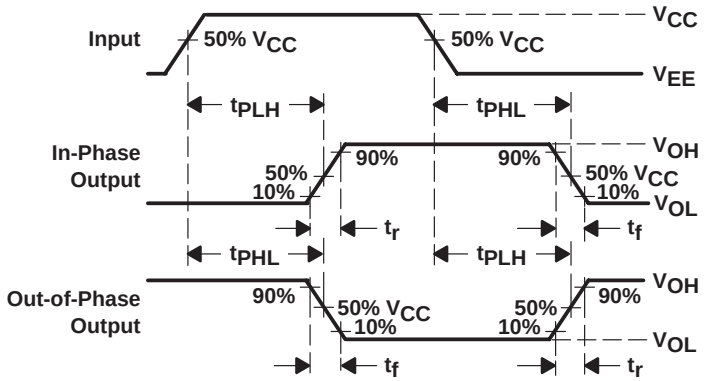
Figure 6. Switch OFF Signal Feedthrough Test Circuit

PARAMETER MEASUREMENT INFORMATION

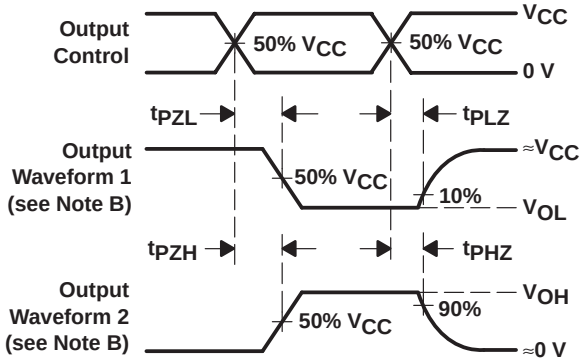


LOAD CIRCUIT

PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd}		Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure 7. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

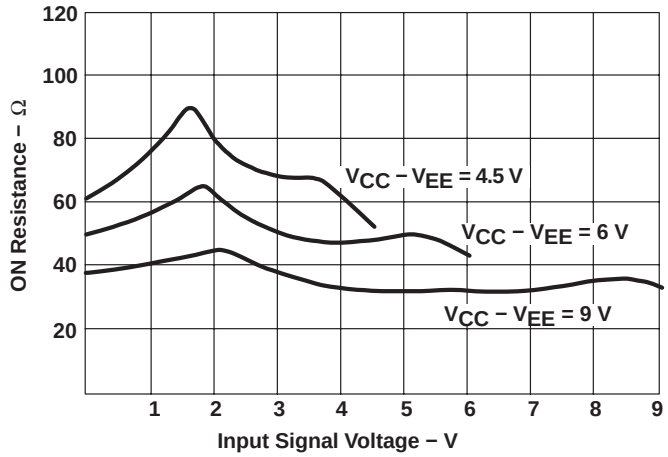


Figure 8. Typical ON Resistance vs Input Signal Voltage

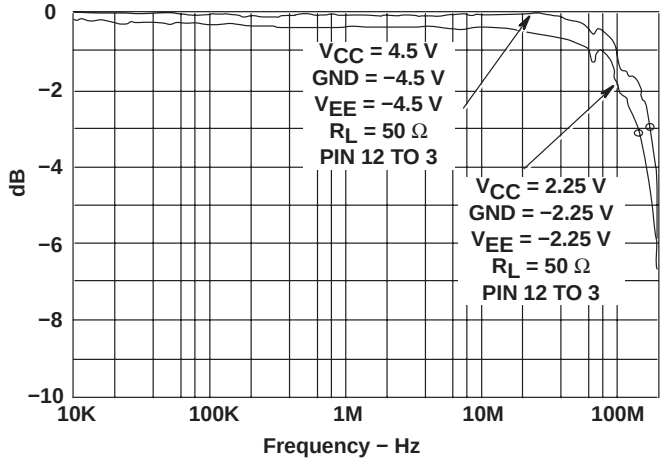


Figure 9. Channel ON Bandwidth

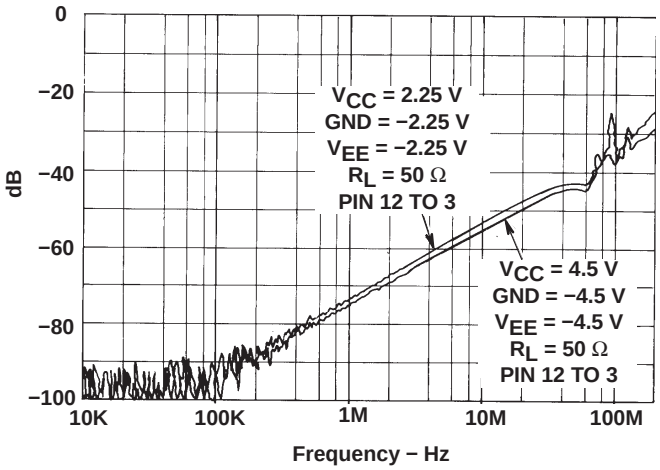


Figure 10. Channel OFF Feedthrough

PACKAGING INFORMATION

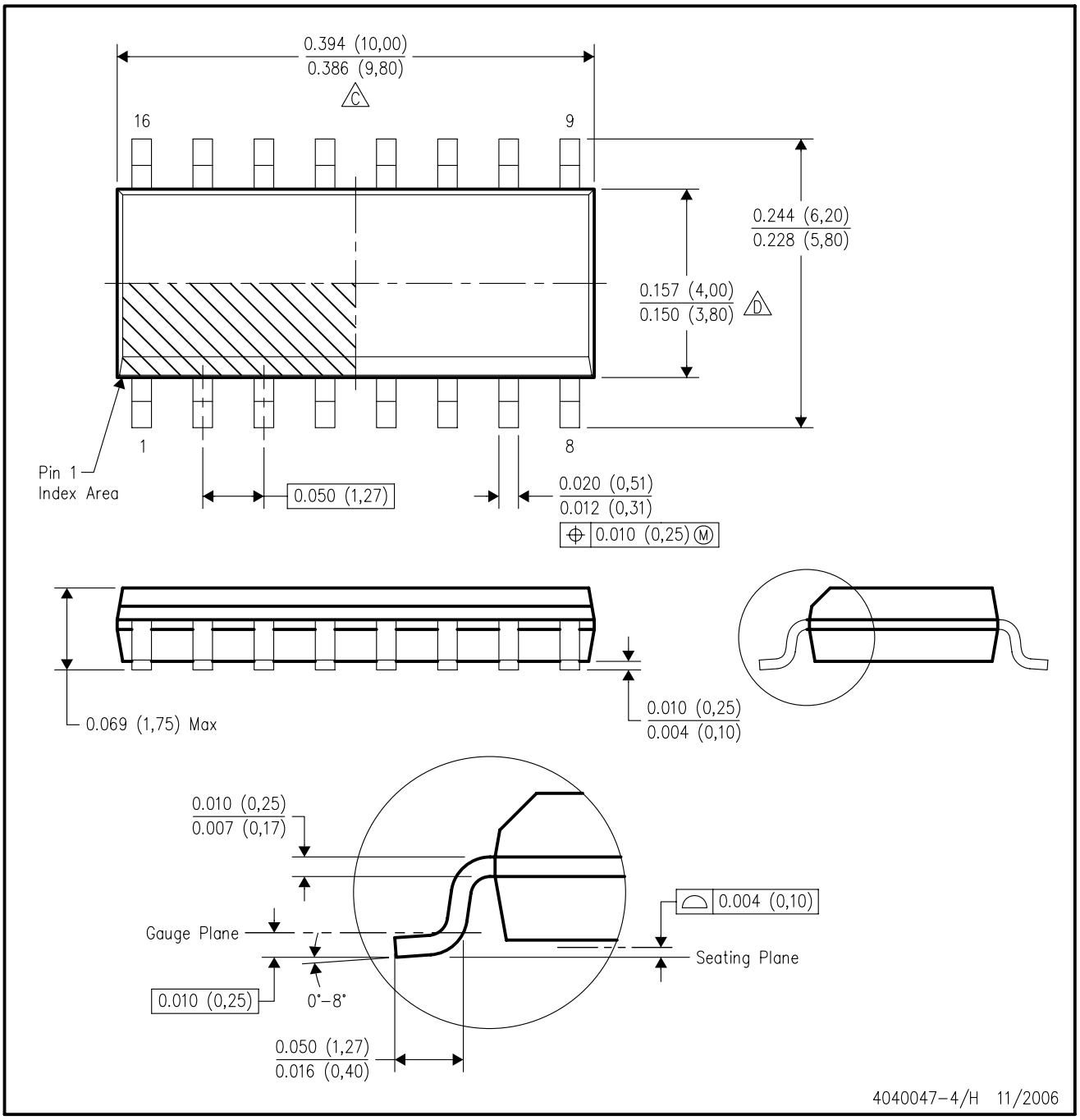
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
CD74HC4051QM96Q1	ACTIVE	SOIC	D	16	2500	Pb-Free (RoHS)	CU NIPDAU	Level-2-250C-1 YEAR/ Level-1-235C-UNLIM
CD74HC4051QPWRQ1	ACTIVE	TSSOP	PW	16	2000	Pb-Free (RoHS)	CU NIPDAU	Level-1-250C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

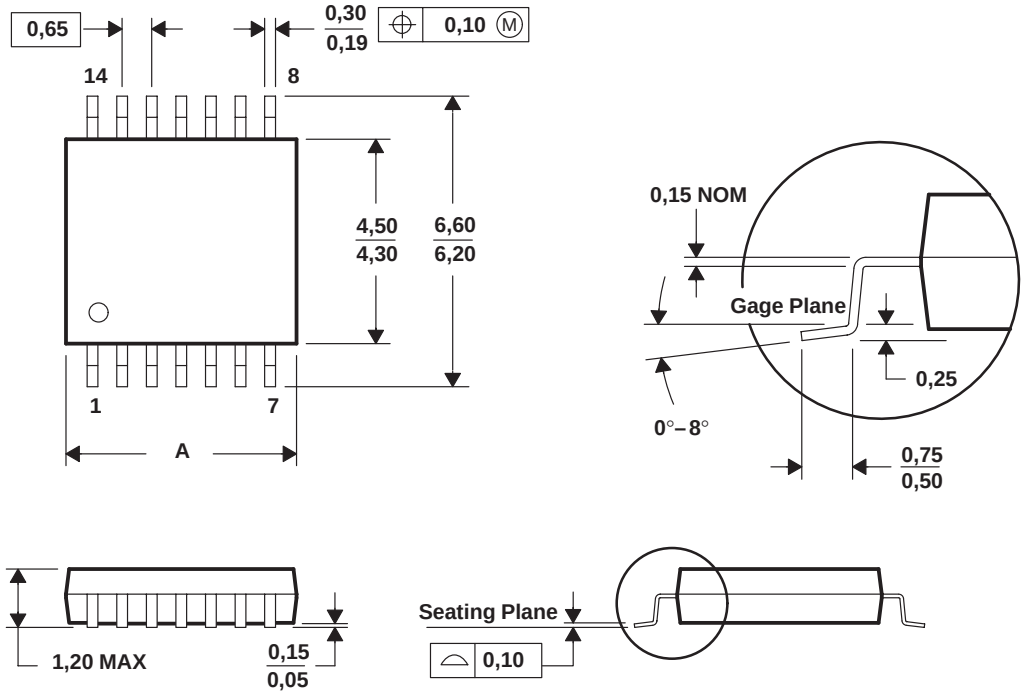
D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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